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TITLE: Clock synchronous memory embedded semiconductor integrated circuit device

Detailed Description Text (98):
FIG. 21 schematically shows a whole structure of a semiconductor integrated circuit device according to an embodiment 3 of the invention. The semiconductor integrated circuit device shown in FIG. 21 differs from the semiconductor integrated circuit device shown in FIG. 13 in the following point. The device is provided with a compression circuit 4j which compresses data of 256 bits issued from latch circuit 4e into data of 1 bits, and a latch 4k which transfers and applies a signal of 1 bit from compression circuit 4j to a pad 8p in accordance with test clock signal ETCLK. Structures other than the above are the same as those shown in FIG. 13. Corresponding portions bear the same reference numbers, and will not be described below.

Detailed Description Text (107):
The semiconductor integrated circuit device described above contains the synchronous memory which takes in the data and the external signal at the rising or falling edge of the clock signal. However, the invention can be applied to a synchronous memory called a DDRSDRAM, which performs input and output of data in synchronization with the rising and falling edges of the clock signal, and takes in external signals (control signal and address signal) at one of the edges of clock signal. By providing two latch circuits at the write data transmission path and the read data transmission path such that these latch circuits on the two paths are selected in synchronization with the rising and falling of the clock signal, data transfer can be performed in synchronization with the rising and falling of the clock signal, and writing/reading of the data at DDR (double data rate) can be performed. Since the control signal and address signal are merely transferred in synchronization with one of the edges of clock signal, the same structure as those in the foregoing embodiments 1 to 3 can be used.

CLAIMS:

14. The semiconductor integrated circuit device according to claim 3, wherein

said synchronous direct memory access circuit further includes means for compressing the data of multiple bits received from said data taking means into data of one bit for outputting in synchronization with said test clock signal.